University of Mumbai

Program: Computer Engineering
Curriculum Scheme: Rev 2016
Examination: TE Semester V
Course Code: CSC501 and Course Name: Microprocessor

Time: 2 hour Max. Marks: 80

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	The instruction that is used to transfer the data from source operand to destination operand is
Option A:	branch instruction
Option B:	arithmetic/logical instruction
Option C:	string instruction
Option D:	data copy/transfer instruction
2.	In which mode do all the Ports of the 8255 PPI work as Input-Output units for data transfer?
Option A:	BSR mode
Option B:	Mode 0 of I/O mode
Option C:	Mode 1 of I/O mode
Option D:	Mode 2 of I/O mode
3.	If any interrupt request given to an input pin cannot be disabled by any means then the input pin is called
Option A:	maskable interrupt
Option B:	Non maskable interrupt
Option C:	maskable interrupt and non maskable interrupt
Option D:	maskable interrupt or non maskable interrupt
4.	The instruction, MOV AX, [2500H] is an example of
Option A:	immediate addressing mode
Option B:	indirect addressing mode
Option C:	direct addressing mode
Option D:	register addressing mode
5.	The type of execution which means that the CPU should speculate which of the next instructions can be executed earlier is
Option A:	speculative execution
Option B:	out of turn execution
Option C:	dual independent bus
Option D:	multiple branch prediction
6.	An interrupt breaks the execution of instructions and diverts its execution to
Option A:	Interrupt service routine
Option B:	Counter word register
Option C:	Execution unit
Option D:	control unit

7.	The contents of a base register are added to the contents of index register in
Option A:	indexed addressing mode
Option B:	based indexed addressing mode
Option C:	relative based indexed addressing mode
Option D:	based indexed and relative based indexed addressing mode
8.	How many data lines in total are there in the 8255 PPI IC?
Option A:	8 data lines
Option B:	16 data lines
Option C:	32 data lines
Option D:	64 data lines
9.	The unit that is used to implement the multiple branch prediction in Pentium is
Option A:	control unit
Option B:	bus interface unit
Option C:	branch target buffer
Option D:	branch instruction register
10.	The Programmable interrupt controller is required to
Option A:	handle one interrupt request
Option B:	handle one or more interrupt requests at a time
Option C:	handle no interrupt request
Option D:	handle one or more interrupt requests with a delay
11.	The pin that disables all the DMA channels by clearing the mode registers is
Option A:	MARK
Option B:	CLEAR
Option C:	RESSET
Option D:	READY
12.	The IOW (active low) in its slave mode loads the contents of a data bus to
Option A:	8-bit mode register
Option B:	16-bit mode register
Option C:	upper/lower byte of 16-bit DMA address register
Option D:	terminal count register
13.	The paging unit is enabled only in
Option A:	virtual mode
Option B:	addressing mode
Option C:	protected mode
Option D:	Unprotected mode
14.	For a single task in protected mode, the 80386 can address the virtual memory of
Option A:	64 MB
Option B:	32 TB
Option C:	64 TB
Option D:	32 GB
15.	Which of the following instruction is not valid?
Option A:	MOV AX, BX

Option B:	MOV DS, 5000H
Option C:	MOV AX, 5000H
Option D:	PUSH AX
16.	The following statement of ALP is an example of MOV EBX, [EDX*4] [ECX].
Option A:	base scaled indexed mode
Option B:	scaled indexed mode
Option C:	indexed mode
Option D:	based scaled indexed mode with displacement mode
17.	Which of the following is not a data copy/transfer instruction?
Option A:	MOV
Option B:	PUSH
Option C:	POP
Option D:	DAS
18.	The linear address is calculated by
Option A:	effective address + segment base address
Option B:	effective address - segment base address
Option C:	effective address + physical address
Option D:	effective address - physical address
19.	In fetch-decode unit, the number of parallel decoders that accept the stream of fetched instructions and decode them is
Option A:	1
Option B:	2
Option C:	3
Option D:	4
20.	The operation that can be performed on segments in 80386 real mode is
Option A:	Read
Option B:	Write
Option C:	execute
Option D:	overlapped

Q2 **(20 Marks Each)**	
	Solve any Two Questions out of Three **10 marks each**
i.	Explain segmentation of 8086 microprocessor. Give its advantages.
ii.	Draw and explain the block diagram of 8257 DMA controller.
iii.	Draw and explain the architecture of Pentium processor.

Q3. **(20 Marks Each)**	
	Solve any Two Questions out of Three **10 marks each**
i.	Explain minimum mode configuration of 8086 microprocessor
ii.	Draw and explain the block diagram of PIT 8253.
iii.	Differentiate Real Mode, Protected Mode and virtual 8086 mode of 80386 microprocessor